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R. Dorn

S/N 09/208105

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sakamoto, et al	Examiner:	O. NADAV
Serial No.:	09/208105	Group Art Unit:	2811
Filed:	November 25, 1998	Docket No.:	10233.81USW1
Title:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREFOR		

CERTIFICATE UNDER 37 CFR 1.6(d):
I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on June 24, 2002.
By: Lisa Dorn
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AMENDMENT UNDER RULE 111

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Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Official Action dated February 22, 2002, please amend this application as follows:

IN THE SPECIFICATION

Next, a method for manufacturing the IGBT 1 will be described. The manufacturing process similar to an ordinary IGBT are carried out until forming the source region 23. In other words, the substrate 2 is formed by consecutively forming the n^+ type later 5 on the drain layer 3 and the n^- type layer 7 thereon as shown in Fig. 4A. Thereafter, the gate oxidation layer 15 and the gate electrode 17 are formed successfully as shown in Fig. 4B. Ion implantation of P-type impurities is carried out by using the gate electrode 17 as a mask. Further, N-type impurities are implanted ionically by using both resist layers 81 formed on the gate oxidation layer 15 and gate oxidation layers 17 as a mask as shown in Fig. 4C. The base region 21 with a P^+ type and a pair of the source regions 23 located in the base region 21 are formed simultaneously by carrying out thermal treatment as shown in Fig. 5A.